W. M. KECK OBSERVATORY

Thirty Meter Telescope Project
A Polar Coordinate Detector for LGS AO
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INTRODUCTION

The current design for the TMT AO system utilizes multiple Shack-Hartmann (SH) wavefront sensors in conjunction with multiple guide star lasers. The large number of subapertures and perspective elongation of the LGS image present two significant challenges to SH wavefront sensor design.

Each of the TMT LGS wavefront sensors will have about 3,000 subapertures in the first light 60 x 60 AO system, and about 12,000 subapertures in the second-generation 120 x 120 AO system. The conventional approach to SH wavefront sensor design is to use a CCD with a pixel array that covers the entire wavefront sensor focal plane. For the TMT this would require a CCD approaching the size of typical science detectors, and achieving the desired signal to noise ratio and read out speeds would be very difficult. Additionally, the conventional approach does not offer the possibility of tracking the image of a pulsed laser spot as it transits the sodium layer, a technique that has the potential to mitigate the significant perspective elongation and range uncertainty of the LGS image that occurs with a thirty meter aperture.

This document describes the approach that we believe will lead to the development of detectors suitable for the LGS AO wavefront sensing needs of the TMT. This approach is based on the work currently underway in a development project led by the W. M. Keck Observatory and funded by the Adaptive Optics Development Program (AODP).

CURRENT WORK

In our current AODP project, “Next Generation Optical Detectors for Wavefront Sensing” we are prototyping a CCD based on a “novel pixel geometry”. This CCD makes use of small “islands” of pixels within each subaperture, interconnected by multiplexers to bring the video signal from each of the pixel islands to the output pins of the device. The pixel islands are rectangular in shape with the major axis of each pixel island oriented along radial lines from the center of projection for the guide star laser (hence the name “polar coordinate detector”). This means that the elongation direction of the LGS image in each subaperture will be along the major dimension of the rectangular pixel island.

The AODP prototype (referred to as the “phase 2 device”) will demonstrate all of the CCD design features required for the TMT LGS AO wavefront sensor, using 30 x 30 subapertures corresponding to one quadrant of a 60 x 60 subaperture device designed for center projection of the guide star laser[1]. The design will be suitable for use with both pulsed lasers and CW lasers. We are planning to complete this prototype development at the end of calendar 2006.

DEVELOPMENT APPROACH

Our proposed development approach would utilize the CCD design and fabrication capabilities of the Lincoln Laboratory of the Massachusetts Institute of Technology (MIT/LL). Barry Burke of MIT/LL would lead the CCD design in collaboration with Sean Adkins of WMKO who would serve as the project manager for the CCD development and provide the technical interface with the TMT project and the AO system designers. Sean Adkins would also be available to collaborate with the HIA in the development of the read out electronics and device packaging for the LGS AO wavefront sensors.

The polar coordinate detector design will be based on the phase 2 device from our AODP development. The phase 2 imager and frame store design is based on proven MIT/LL designs including the phase 1 CCD from our AODP project. We are also planning to use the low noise planar JFET output amplifier developed for the phase 1 CCD. The multiplexing logic in the phase 2 device will be based on the multiplexing logic developed for the Pan-STARRS orthogonal transfer CCD, and the device will also use the silicon on insulator process (also used for the Pan-STARRS devices) to allow multiple layers of interconnect metallization.

The polar coordinate CCD requires a significant amount of logic to implement multiplexing for the frame store clock signals and the video outputs. In addition matching the imager clock rates to the apparent motion of the LGS pulse image requires multiple imager clock signals across the CCD. In our phase 2 prototypes we are implementing all of the required logic in the NMOS process used to implement the pixel arrays. We are concerned that this may not be practical for larger devices due to speed and power dissipation concerns.

An alternative that is better suited to the polar coordinate CCD is the use of a CMOS process to implement the multiplexing and clock logic and mating this CMOS device to a CCD device providing the imager, frame store and output amplifier for each subaperture. The CCD would be a thinned, back illuminated device with front side connections arranged for direct interconnection to the CMOS multiplexer. Both devices would utilize silicon substrates, avoiding problems with differential thermal expansion, and vertical interconnections between the two devices will be made using direct molecular bonding and vias instead of the “bump bonds” commonly used in the fabrication of infrared detector arrays.

In our AODP project we employed a “wafer of opportunity” approach that allowed us to piggyback our small prototype designs on wafers carrying major designs for other MIT/LL customers. This allowed us to fabricate prototype devices at very low cost, but left our schedule at

[1] Although we understand the current design of the TMT LGS AO system uses center projection, all of the concepts described here are also applicable to the design of a CCD for use with offset projection.

the mercy of the primary wafer customer and any process development or schedule issues that the primary program encountered. For the TMT project we propose to make our own full wafer run, allowing much better control of the development and delivery schedule.

CCD Development

The CCD portion of the polar coordinate wavefront sensor will directly use the imager and frame store design from the phase 2 AODP project CCD. For the 60 x 60 devices the layout of one quadrant and each of the subapertures within that quadrant will be identical to the phase 2 prototype. This layout will simply be rotated and repeated to produce the other three quadrants. For the 120 x 120 devices the design will be scaled to utilize a smaller pixel size. In both cases we would only implement the active subapertures as discussed in our design report on the phase 2 CCD.

An overall view of the proposed 60 x 60 subaperture device layout is shown in Figure 1.

We believe that both 60 x 60 and 120 x 120 devices can be implemented on a single wafer run. At least 12 wafers will be fabricated, with each carrying approximately 30 of the 60 x 60 devices and 20 of the 120 x 120 devices. Even with a 10% yield for fully functional devices this will deliver 24 of the 120 x 120 devices and 36 of the 60 x 60 devices. Based on past experience we expect to achieve yields higher than 10%.

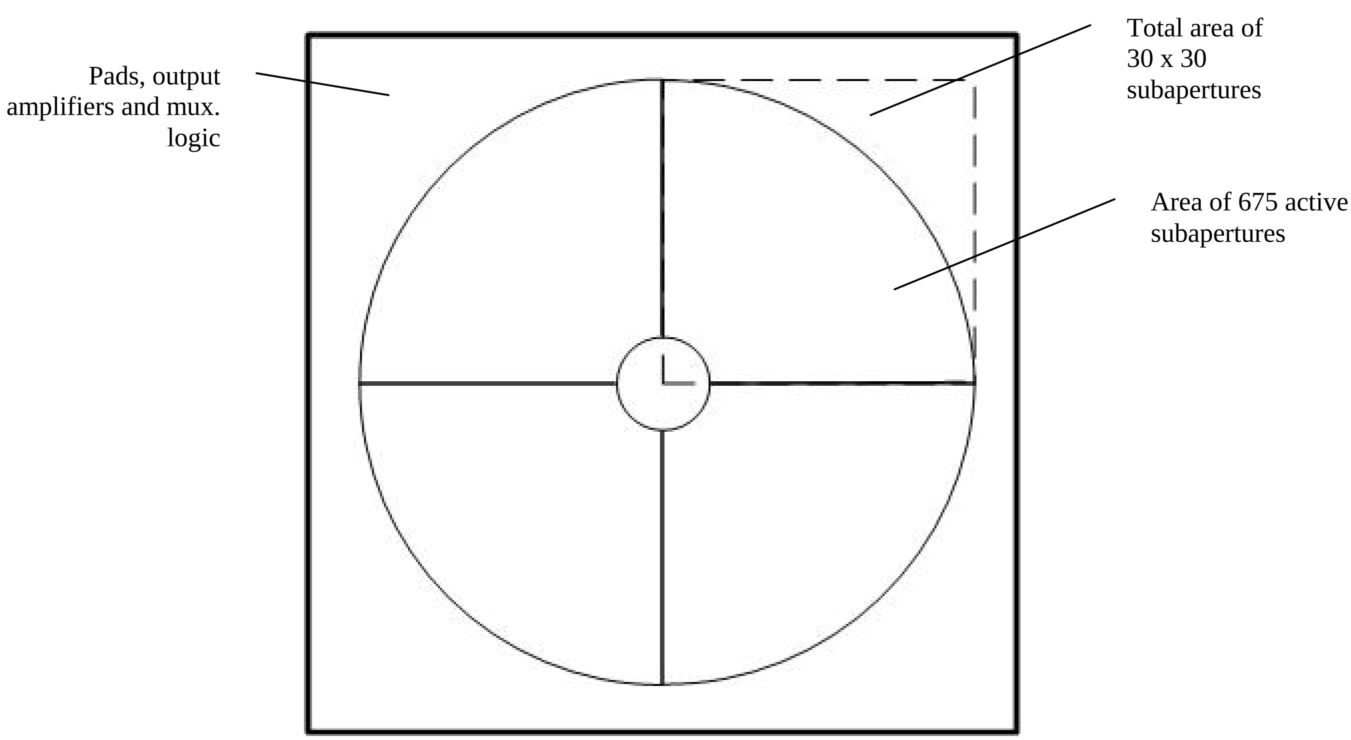

Figure 1 : 60 x 60 Subaperture Device Layout

Multiplexer Development

The CMOS multiplexers will also be fabricated using a MIT/LL process. In this case we may choose to share a wafer run (paying a portion of the total costs) with another project if a compatible schedule can be identified. It would be desirable to fabricate the 60 x 60 multiplexers first so that test results from the 60 x 60 devices can be used to optimize the design of the 120 x 120 multiplexers. If necessary this approach also allows a second run of 60 x 60 multiplexers on a wafer carrying the run of 120 x 120 multiplexers.

We anticipate good yields from the CMOS process and a minimum of schedule uncertainty since it is a well-characterized process.

Readout Electronics

In addition to the development of the polar coordinate detector a suitable read out system will be required. Even with video multiplexing the 60 x 60 device will require approximately 130 video outputs if a 1500 Hz frame rate is desired. There is a high level of integration readout system being developed at the IfA for the Pan-STARRS project and this design may be available for adaptation to the polar coordinate CCD.

The development of a suitable readout electronics system and a detector package (hermetic TEC or Cryotiger dewar) for the polar coordinate CCD will be an important part of developing a complete solution for integration into the TMT LGS AO system.

DEVELOPMENT SUMMARY

In conclusion we propose the following development activities:

1. CCD design and fabrication for a wafer carrying both 60 x 60 and 120 x 120 polar coordinate detector arrays.
2. CMOS multiplexer development, using a shared wafer for a 60 x 60 multiplexer.
3. Prototype testing of a 60 x 60 polar coordinate detector.
4. Fabrication of a CMOS multiplexer wafer run carrying both 60 x 60 and 120 x 120 multiplexers.

A timeline of approximately 24 months will be required for steps 1 through 3, with an additional 12 to 18 months needed for step 4.